



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/824,897

04/15/2004

Srinivas Cheedela

15143US01

7572

23446 7590 06/02/2009
MCANDREWS HELD & MALLOY, LTD
500 WEST MADISON STREET
SUITE 3400
CHICAGO, IL 60661

EXAMINER

ROBERTS, JESSICA M

ART UNIT

PAPER NUMBER

2621

MAIL DATE

DELIVERY MODE

06/02/2009

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 02/25/2009 have been fully considered but they are not persuasive.

As to Applicants argument regarding Yuan was filed on Aug. 6, 2004, after the present application. Although, Yuan claims priority to provisional patent application, 60/499,223, 60/496,508, and 60/493,509. Assignee respectfully submits that the portions that are relied upon by Examiner, [0037], [0046], [0108], figs. 1, 4, 6, and 8 are not found in the provisional patent applications, 60/499,223, 60/493,508, and 60/493,509. Accordingly the Assignee respectfully traverses the rejection to claims 1-4 because Yuan is not prior art for the claimed invention.

The Examiner respectfully disagrees. Provisional Application 60/499,223 in which Yuan claims priority discloses and more than fairly suggests to provide support for video and audio applications differing standards and formats without significant hardware overhead, (see 1. Challenges (pg. 2 line 1-9)) which provide support for paragraph [0037]. Paragraph [0108] is more than fairly suggested and taught in the Provisional Application 60/499,223 (see 2.2 Partition for Multi-standard Video Encode System, pg. 5 figs. 5-8). Figs. 1, 4, 6, and 8 are more than fairly suggest and taught by 2.1 Partition for Multi-standard Video Decode System, pg. 2 and figs. 1-4. Therefore, Yuan is competent prior art, as the effective filing date of the reference being that of the provisional application which falls before Applicants filing date.

Status of Claims

2. Claims 1, 2 and 4-10 are presently pending and claim 3 has been **cancelled** by applicants submission filed on 09/15/2008.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fimoff et al., US-6, 510,178 in view of Yuan et al., US-2005/0094729 A1 and further in view of Applicants Admitted Prior Art (AAPA).

6. Regarding claim 1, Fimoff teaches a decoder for decoding macroblocks, said video decoder comprising: a processor (fig. 5, decoder 100) for decoding a set of parameters, said set of parameters comprising motion vectors indicating reference pixels associated with the macroblock (abstract); a motion vector address computer for calculating addresses associated with motion vectors (column 29 line 34-49); a pixel

Art Unit: 2621

reconstructor for reconstructing pixels from the macroblocks, the pixel reconstructor operable to reconstruct pixels from macroblocks encoded in accordance with a plurality of standards (column 6 line 50-58); said pixel reconstructor further comprising: a macroblock input buffer for storing the reference pixels that are fetched from the frame buffer by the video request manager at the addresses calculated by the motion vector address computer (Fimoff teaches a method of reconstructing pixel blocks from P and B DCT coded blocks comprises the following steps: a) selecting reference pixel from a memory in response to a motion vector, column 6 line 50-55. Further, a motion vector translator 150 translates the received full resolution motion vector into a low resolution motion vector as previously described. The low resolution motion vector is then converted into reference picture memory addresses for supply to the memory 106, column 29 line 36-41. The reference pixels read from the memory 106 by the addresses from the motion vector translator 150 are supplied to a horizontal prediction filter, column 29 line 44-46. Therefore, it is clear to the examiner that Fimoff teaches a buffer to store the reference pixels that are addressed by the motion vector address computer, which reads upon the claimed limitation).

Fimoff does not explicitly teach a frame buffer for storing past and future reference pictures; a video request manager for fetching a block of reference pixels at the addresses calculated by the motion vector address computer; the reference pixels are fetched from the frame buffer and a register for storing a portion of the reference pixels that are fetched from the frame buffer by the video request manager at the addresses calculated by the motion vector address computer; and wherein the register,

macroblock, input buffer, and frame buffers are separate, a frame buffer for storing past and future reference pictures.

However Yuan teaches a frame buffer for storing past reference pictures (fig. 8); a processor-based system for encoding and decoding a plurality of standards for compression ([0037], [0108] and fig. 1, 4, 6, and 6). Yuan further teaches the reference pixels are located in frame buffer (fig. 8). The examiner notes that in order to retrieve the reference pixels from the frame buffer would necessitate the use of retrieve or call command or video request manager); the reference pixels are fetched from the frame buffer (fig. 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Yuan with Fimoff for allowing for support video and audio application differing standards and formats without significant hardware overhead, Yuan [0037].

Fimoff (modified by Yuan) as a whole is silent in regards to a register for storing a portion of the reference pixels that are fetched from the frame buffer by the video request manager at the addresses from the frame buffer that were calculated by the motion vector address computer.

However, APPA a register for storing a portion of the reference pixels that are fetched from the frame buffer that are fetched from the frame buffer by the video request manager at the addresses from the frame buffer that were calculated by the motion vector address computer (During decoding, the motion vectors are used to retrieve the reference pixels. The reference pixels are retrieved from a memory storing

the reference frame. The memory storing the reference frame is known as a frame buffer. A motion vector address computer determines the appropriate addresses storing the reference pixels for a macroblock, based on motion vectors, [0007]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Fimoff (modified by Yuan) with AAPA for providing efficient image processing.

Fimoff (modified by Yuan and AAPA) as a whole have the majority of the features of claim 1, but still fails to teach wherein the register, macroblock input buffer, and frame buffers are separate. However, it would have been an obvious modification readily apparent to one of ordinary skill in the art at the time of the invention since it entails to separate the register, macroblock input buffer, and frame buffers, which is merely to make separable, a distinction which the courts have already ruled against Nerwin v. Erlichman, 168 USPQ 177, 179 (PTO Bd. of Int. 1969).

Regarding claim 2, Fimoff (modified by Yuan) as a whole teaches everything as claimed above, see claim 1. Fimoff is silent in regards to of Fimoff and Yuan as a whole further teach wherein the plurality of standards comprises MPEG-2 and AVC.

However, Yuan teaches wherein the plurality of standards comprises MPEG-2 and AVC (Yuan, Fig. 4, 6, and 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Yuan with Fimoff for allowing for

support video and audio application differing standards and formats without significant hardware overhead, Yuan [0037].

Regarding claim 4, Fimoff (modified by Yuan) as a whole teaches everything as claimed above, see claim 1. Fimoff is silent in regards to the wherein the pixel reconstructor (Fimoff and Yuan, decoder) comprises; a data path for outputting another portion of the reference pixels.

However, Yuan teaches wherein the pixel reconstructor (decoder) comprises; a data path for outputting another portion of the reference pixels (Yuan discloses the reference pixels are output to the motion compensation unit, fig.8, 800. The examiner notes that the frame buffer contains the reference frames, and reference frames are composed of reference pixels. Further, the reference frames are output to the motion compensation unit 812). More so, to output the reference pixels from the frame buffer, would necessitate the use of a data path.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teaching of Yuan with Fimoff for allowing for support video and audio application differing standards and formats without significant hardware overhead, Yuan [0037].

7. Claims 5-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Diaz et al., US- 5,920,353 in view of Applicants Admitted Prior Art (AAPA) in view of Moon US-6, 222,467 and further in view of Ueda et al., US-2002/0009287.

8. Regarding claim 5, Diaz teaches a pixel reconstructor (fig. 3) for decoding macroblocks, said pixel reconstructor comprising: a macroblock input buffer (FIFO, fig.

3); a multiplexer connected to the macroblock input buffer (MUX, fig. 3). Diaz is silent in regards to the macroblock input buffer for storing reference pixels that are referenced by at least one motion vector, a register connected to the multiplexer for storing a portion of the reference pixels that are referenced by the at least one motion vector; and a data path connected in parallel to the register.

However, APPA a register for storing a portion of the reference pixels that are referenced by the at least one motion vector (During decoding, the motion vectors are used to retrieve the reference pixels. The reference pixels are retrieved from a memory storing the reference frame. The memory storing the reference frame is known as a frame buffer. A motion vector address computer determines the appropriate addresses storing the reference pixels for a macroblock, based on motion vectors, [0007]).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Fimoff (modified by Yuan) with AAPA for providing efficient image processing.

Diaz (modified by AAPA) is silent in regards to a register connected to multiplexer, and a data path connected in parallel to the register; a macroblock input buffer for storing reference pixels that are referenced by at least one motion vector.

However, Moon discloses multiple registers connected to more than one multiplexer (first-sixth registers, fig. 3 and first – second multiplexers). Further discloses by Moon is that the registers have common pathways between the registers and multiplexers (fig. 3). Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the decompression device of Diaz (modified

by AAPA) with the teaching of Moons' multiple registers and multiplexers to provide a more efficient decoder that increases the speed of the video decoder, bitstream decoder and the operating clock frequency (Moon, column line 31-47).

Diaz (modified by AAPA and Moon) is silent in regards to a macroblock input buffer for storing reference pixels that are referenced by at least one motion vector.

However, Ueda teaches a macroblock input buffer for storing reference pixels that are referenced by at least one motion vector (When a macroblock output from the decoder 15 needs motion compensation, the motion compensation circuit 16 reads the reference pixel data from the video buffer in the buffer via the buffer control circuit 123 in accordance with the prediction vector output from the decoder 15. The obtained reference pixel data is added to pixel data supplied by from the decoder 15 thereby performing motion compensation [0058]. Since Ueda discloses reference the pixels are read from the video buffer, and are supplied to the decoder thereby performing motion compensation, and motion compensation produces a motion vector, therefore, it is clear to the examiner that Ueda teaches to a macroblock buffer that stores reference pixels that are referenced by at least one motion vector.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Ueda with Diaz (modified by Moon) for more efficient image processing.

Regarding claim 6, Diaz (modified by AAPA, Moon, and Ueda) as a whole further teaches a macroblock input buffer register connected to the multiplexer (Moon, first

register; fig. 3). Further Moon discloses registers first through second connected to the second multiplexer.

Regarding claim 7, Diaz (modified by AAPA, Moon, and Ueda) as a whole further teaches another multiplexer connected to the register ((Moon, second register; fig. 3). Further Moon discloses registers first through second connected to the second multiplexer.

Regarding claim 8, Diaz (modified by AAPA, Moon, and Ueda) as a whole further teaches a bypass path connected to the macroblock input buffer and the another multiplexer, said bypass path bypassing the multiplexer and the multiplexer input buffer register (Moon discloses where the data from the second register can either be received by either the first or second multiplexer from the variable length decoder, fig. 3).

Regarding claim 9, Diaz (modified by AAPA, Moon, and Ueda) as a whole further teach to reconstruct pixels from macroblocks encoded in accordance to a plurality of standards (Moon discloses MPEG-1, MPEG-2, H.261, and H.263; column 6 line 5-7).

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Diaz et al., US- 5,920,353 in view of Applicants Admitted Prior Art (AAPA) in view of Moon US- 6, 222,467 in view of Ueda et al., US-2002/0009287 and in further view of Yuan et al., US-2005/0094729.

10. Regarding claim 10, Diaz (modified by AAPA, Moon and Ueda) as a whole are silent in regards to wherein the plurality of standards comprises MPEG-2 and AVC. However, Yuan teaches this limitation (Yuan, fig. 4, 6, and 8). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the

teachings of Yuan with Diaz (modified by AAPA, Moon, and Ueda) to include the standard of AVC for maximizing flexibility and adaptability of the system, thus allowing for support for video and audio application of different standards and formats without significant hardware overhead (Yuan, [0037]).

Conclusion

3. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSICA ROBERTS whose telephone number is

Art Unit: 2621

(571)270-1821. The examiner can normally be reached on 7:30-5:00 EST Monday-Friday, Alt Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marsha D. Banks-Harold can be reached on (571) 272-7905. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Marsha D. Banks-Harold/
Supervisory Patent Examiner, Art Unit 2621
/Jessica Roberts/
Examiner, Art Unit 2621